CLAIMS

What is claimed is:

1. A method for scheduling access to a device comprising:

tracking a current state of a device;

tracking a count of a number of requests which require a particular state; and

scheduling requests to a device using the current state of the device, the count of the number of requests that have already been scheduled using the current state, a switch point indicating when to switch state, wherein after the count reaches the switch point and there are incoming requests having an alternate state to the current state of the device, switching the state of the device to process incoming requests.

2. The method as set forth in claim 1, further comprising configuring the switch point.

3. The method as set forth in claim 2, wherein the switch point is adjustable by software.

4. The method as set forth in claim 2, wherein the switch point is dynamically configurable.

5. The method as set forth in claim 1, wherein the device is a dynamic random access memory (DRAM) a scheduler type is selected from the group consisting of a DRAM bus turnaround scheduling, DRAM page scheduling and DRAM physical bank switching.

6. A bus scheduler comprising:

an input configured to receive at least one incoming request, each request indicating a bus direction;

a switch point;

an indicator of a current bus direction

a count of requests processed using the current bus direction;

logic configured to switch the direction of the bus to process incoming requests wherein after the count reaches the switch point and there are incoming requests having the direction opposite to the current direction of the device bus, switching the direction of the device bus.

7. The bus scheduler as set forth in claim 6, wherein the switch point is configurable.

8. A scheduler comprising:

a switch point;

a current device state;

a count;

logic configured to determine an updated device state using the switch point and count such that when the count crosses a threshold of the switch point, the device state is changed; and

scheduling access requests to the device using the updated device state.

9. The scheduler as set forth in claim 8, wherein the switch point is dynamically configurable.

10. The scheduler as set forth in claim 8 wherein the device comprises a bus and the device state comprises a bus direction, said scheduling dependent upon the bus direction.

11. The scheduler as set forth in claim 8, wherein the device is a dynamic random access memory (DRAM) and scheduling is selected from the group consisting of DRAM bus turnaround scheduling, DRAM page scheduling and DRAM physical bank switching.

12. The scheduler as set forth in claim 6, wherein the switch point is software configurable.

13. The scheduler as set forth in claim 8, wherein the device comprises a DRAM with multiple pages and the device state comprises the identity of at least one open page, said scheduling dependent on the at least one page opened.

14. The scheduler as set forth in claim 8, wherein the device comprises a DRAM with multiple physical banks and the device state comprises the last accessed physical bank, said scheduling dependent on the last accessed physical bank